AMENDMENTS TO CLAIMS

1. (Currently Amended) An oscillator circuit comprising:

a relaxation oscillator circuit;

a first current source for establishing a first reference voltage for use in causing said relaxation oscillator circuit to operate in a first power mode to generate a clock of a first accuracy;

a second current source for establishing a second reference voltage for use in causing said relaxation oscillator circuit to operate in a second power mode to generate a clock of a second accuracy, wherein said first current source is not operable to establish said second reference voltage; and

a control coupled to said first current source and said second current source for switching between said first power mode and said second power mode, wherein said relaxation oscillator circuit generates a clock signal operating at a frequency that is substantially the same in both said first power mode and said second power mode.

2. (Original) The oscillator circuit as recited in Claim 1 wherein said first current source supplies a larger current than said second current source such that said first reference voltage is more accurate than said second reference voltage.

3. (Original) The oscillator circuit as recited in Claim 1 wherein said first reference voltage is established across a resister.

4. (Original) The oscillator circuit as recited in Claim 1 wherein said second reference voltage is established across a diode-connected field effect transistor.

5. (Previously Presented) The oscillator circuit as recited in Claim 1 further comprising trimmable current sources operable to control a current charging a capacitor of said relaxation oscillator circuit to account for process variation in said capacitor, said current charging said capacitor for controlling a frequency of said relaxation oscillator.

6. (Previously Presented) The relaxation oscillator circuit as recited in Claim 5 wherein said trimmable current sources are digitally controlled.

7. (Original) The relaxation oscillator circuit as recited in Claim 1 wherein said first current source generates a current of 2 micro amps.

8. (Original) The relaxation oscillator circuit as recited in Claim 1 wherein said second current source generates a current of 100 nano amps.

9. (Currently Amended) A microcontroller comprising:

a bus;

a processor coupled to said bus;

a memory unit coupled to said bus;

a plurality of input/output pins; and

a timer circuit coupled to said bus for performing a timing function, said timer circuit comprising a relaxation oscillator circuit having a first power mode associated with a first current source and a second power mode associated with a second current source wherein said relaxation oscillator circuit generates a clock signal operating at a frequency that is substantially the same in both said first power mode and said second power mode, said first power mode and said second power mode being switchable under a control, wherein said relaxation oscillator circuit comprises:

said first current source coupled to said control for establishing a first reference voltage for use in causing said relaxation oscillator to operate in a first power mode to generate a clock of a first accuracy, wherein said first current source is not used during said second power mode; and

said second current source coupled to said control for establishing a second reference voltage for use in causing said relaxation oscillator to operate in a second power mode to generate a clock of a second accuracy.

10. (Cancelled)

11. (Original) The microcontroller as recited in Claim 9 wherein said first current source is operable to supply a larger current than said second current source such that said first reference voltage is more accurate than said second reference voltage.

12. (Original) The microcontroller as recited in Claim 9 wherein said first reference voltage is established across a resister.

13. (Original) The microcontroller as recited in Claim 9 wherein said second reference voltage is established across a diode-connected field effect transistor (FET).

14. (Previously Presented) The microcontroller as recited in Claim 9 further comprising digitally trimmable current sources coupled to said relaxation oscillator circuit, said digitally trimmable current sources operable to control a current charging a capacitor of said relaxation oscillator circuit to account for process variation in said capacitor, said current charging said capacitor for controlling a frequency of said relaxation oscillator.

15. (Previously Presented) The microcontroller as recited in Claim 14 wherein said digitally trimmable current sources comprise four trimmable current sources.

16. (Original) The microcontroller as recited in Claim 9 wherein said first current source generates a current of 2 micro amps.

17. (Original) The microcontroller as recited in Claim 9 wherein said second current source generates a current of 100 nano amps.

18. (Original) The microcontroller as recited in Claim 9 wherein said relaxation oscillator circuit generates a clock signal operating at a frequency of substantially 32 KHz.

19. (Currently Amended) In a relaxation oscillator circuit having a first current source for a first power mode and a second current source for a second power mode, a method for generating clock signals comprising:

selecting a switched current source corresponding to a present power mode by switching between said first current source for said first power mode and said second current source for said second power mode, wherein said first current source is not used during said second power mode;

generating a reference voltage based on said switched current source; and

in response to said reference voltage, using said relaxation oscillator circuit to generate a clock signal having an accuracy that depends on said present power mode, wherein said clock signal operates at a frequency that is substantially the same in both said first power mode and said second power mode.

20. (Original) The method as recited in Claim 19 wherein said first current source is operable to supply a larger current than said second current source.

21. (Original) The method as recited in Claim 19 wherein said first power mode is a low power mode.

22. (Original) The method as recited in Claim 19 wherein said second power mode is a very low power mode.

23. (Previously Presented) The method as recited in Claim 19 wherein said relaxation oscillator circuit further comprises digitally trimmable current sources, said digitally trimmable current sources operable to control a current charging a capacitor of said relaxation oscillator circuit to account for process variation in said capacitor, said current charging said capacitor for generating said clock signal.

24. (Previously Presented) The method as recited in Claim 23 wherein said relaxation oscillator circuit comprises four trimmable current sources.

25. (Original) The method as recited in Claim 19 wherein said first current source generates a current of 2 micro amps.

26. (Original) The method as recited in Claim 19 wherein said second current source generates a current of 100 nano amps.

27. (Original) The method as recited in Claim 19 wherein said clock signal operates at a frequency of substantially 32 KHz.